SDC | Software Defined Communication Testbed

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Drexel University's Software Defined Communication Testbed (SDC) seeks to provide a rapid prototyping system for advancing research in spectrum utilization through radio, optical and ultrasonic communication modalities. SDC provides its users a wide range of modular physical (PHY) development flexibility across OFDM based standards as well as the ability to tweak aspects within existing standards. In addition to providing scalability within a common software framework, our design enables and promotes the development of a diverse set of security and timing-aware applications that depend on the availability of an easily reconfigurable framework. SDC's front end interface was built to support various modular transceivers. We are currently focusing our development efforts towards the frequency-agile Nutaq 420X radio board. SDC derives its capability from a full FPGA based SOFDM (Scalable OFDM) baseband implementation designed to give hardware speed with software flexibility through parameters controlled through memory registers from software.

There are several prominent SDRs in the academic community and the Drexel Wireless System Lab (DWSL) has utilized a mix of these platforms for research purposes. However, the majority of SDR platforms that are widely available to the academic and industrial research community have several notable limitations, including:

- Sampling rates and processing capabilities predominantly limited to IEEE 802.11 systems
- Lack of available FPGA fabric and programming flexibility to allow implementation of newest algorithms proposed by the communications and signal processing community
- Exclusive focus on radio-frequency based communications

To address these limitations, using funding from NSF (CNS #0923003 and CNS #0854946), DWSL has developed the SDC Testbed for release to the wireless academic and industrial research community. It is designed to provide a cohesive and affordable hardware/software infrastructure for fast and flexible algorithm development across multiple layers of the communication stack. It currently supports real time FPGA prototyping of OFDM based systems with subcarrier counts varying from 16 to 512, modulation constellation sizes from BPSK to 16QAM, variable coding rates and data rates which can theoretically be modified on a packet to packet basis.

Every module of SDC's core baseband layer is built with controllers specific to its functionality and intelligence that can be modified or scaled during run time. SDC's research oriented framework makes it easy to inject data, control signals, as well as to modify algorithms between modules or even within them, with debug ports extracted across the entire design to test outcomes. Our framework also provides researchers a platform to test and rapidly prototype algorithms in MATLAB and then export to SDC for hardware testing. SDC will enable rapid prototyping of new standards for future communications, where newly developed algorithms can be tested on multiple hardware architectures seamlessly.

Attributes and Applications

- Supports wide range of OFDM symbol sizes making research into adaptive spectral learning and optimization of different communication standards viable on SDC.
- Supports multiple QAM modulation, coding and interleaving rates with the capability to switch or scale the modules associated with these parameters, thereby enabling energy and adaptive bit loading schemes for efficient spectrum utilization.
- Supports switching to a conjugate symmetric processing path to allow for prototyping real, non-complex signaling appropriate for optical communications.
- Supports selective loading of subcarriers to enable NC-OFDM schemes to selectively dodge noisy channels based on Channel State Information (CSI) feedback.
- SDC's co-simulation framework through MATLAB can be used to build and test algorithms and designs to be introduced into the core separately on the host PC, decreasing turnaround times.